EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4956	(341/143,155,144,118,120).CCLS.	USPAT	OR	OFF	2006/07/18 10:47
L2	1021	(341/143,155,144,118,120).CCLS.	US-PGPUB	OR	OFF	2006/07/18 10:47
L3	303	(341/143).CCLS.	US-PGPUB	OR	OFF	2006/07/18 10:48
L4	1	delta sigma current (falling or trailing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:48
L5	0	delta sigma current (falling or trailing) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:48
L6	0	delta sigma current (falling or trailing) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:49
L7	0	delta sigma current (falling or trailing) and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:49
L8	0	delta sigma current (falling or trailing) and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:49
L9	14	delta sigma current (falling or trailing)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:49
L10	0	delta sigma current (falling or trailing) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:49

EAST Search History

L11	0	delta sigma current (falling or trailing) and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:50
L12	353	delta sigma current and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:50
L13	66	delta sigma current and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:50
L14	53	delta sigma current and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:50
L15	58	delta sigma current source dac	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:51
L16	26	delta sigma current source dac and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/07/18 10:51
L17	5	delta sigma current source dac and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/07/18 10:51

Terms used **delta sigma current** Found **161** of **182,223**

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Relevance scale

1 RF circuit design and design methodology: A 1GHz CMOS fourth-order continuous-time bandpass sigma delta modulator for RF receiver front end A/D conversion

K. Praveen Jayakar Thomas, Ram Singh Rana, Yong Lian

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(661.92 KB) Additional Information: full citation, abstract, references

A design and circuit implementation of a CMOS fourth-order continuous-time bandpass *f*s/4 sigma delta modulator is presented. The fully differential architecture of the modulator includes integrated LC resonators with active Q enhancement and return to zero, half return to zero latches to drive the feedback switched current source DACs. The modulator, designed for 0.18μm/1.8V 1P6M CMOS process occupies a total area of 1.8mm^2 dissipating 290mW from a 1.8V power supp ...

2 Low-voltage low-power switched-current circuits and systems

Nianxiong Tan, S. Eriksson

March 1995 **Proceedings of the 1995 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(642.50 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper presents low-voltage low-power switched-current circuits and systems. Novel class AB configuration and common-mode feedforward are the essence. A delay line, memory cell, oversampling A/D converter, and chopper-stabilized oversampling A/D converter were designed and implemented. Measurement results are presented as well.

Keywords: CMOS IC, CMOS analogue integrated circuits, LV switched-current circuits, SI memory cell, analogue processing circuits, analogue storage, analogue-digital conversion, chopper-stabilized oversampling ADC, class AB configuration, common-mode feedforward, delay line, delay lines, feedforward, low-power switched-current circuits, oversampling A/D converter, sampled data circuits, switched current circuits

3 Automatic Synthesis and Simulation of Continuous-Time [Sigma-Delta] Modulators

H. Aboushady, L. de Lamarre, N. Beilleau, M. M. Louërat

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Publisher: IEEE Computer Society
Full text available: pdf(253.26 KB) Additional Information: full citation, abstract, index terms

This paper presents a mixed equation-based and simulation-based design methodology for continuous-time Sigma-Delta modulators from high level specifications down to Layout. The calculation and scaling of the Sigma-Delta coef.cients as well as circuit sizing and layout generation are implemented in the same analog design environment CAIRO+. The design of a complete third order current-mode continuous-time Sigma-Delta modulator is taken as an example to show the effectiveness of the proposed desig ...

4 Poster session 2: An integrated circuit/behavioral simulation framework for continuous-time sigma-delta ADCs
Mohamed El-Nozahi, Yehia Massoud
April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**
Publisher: ACM Press
Full text available: pdf(228.10 KB) Additional Information: full citation, abstract, references, index terms

Predicting the performance of the EΔEΔ analog to digital converters (ADCs) is a computationally expensive task that can take several days for estimating the performance. In this paper, we propose a new circuit/behavioral simulation framework for accurately estimating the performance of CT-EΔ-ADCs. Our framework is based on newly developed simulation-directed macro-models and associated mapping techniques for accurately modeling and simulating the CT-EΔ-ADC ...

Keywords: macro-modeling, sigma-delta, simulation

5 (Special session) presentation + poster disscussion: university design contest: A dynamic element matching circuit for multi-bit delta-sigma modulators
Ryozo Katoh, Shin-ya Kobayashi, Takao Waho
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**
Publisher: IEEE Press , IEEE Press
Full text available: pdf(161.73 KB) Publisher Site Additional Information: full citation, abstract, references

A 30k-gate dynamic element matching circuit for bandpass modulators with a 4-bit quantizer is designed by using 0.35-μm CMOS technology. Second-order bandpass mismatch-shaping algorithm improves the signal-to-noise ratio by ~30dB (~5 bit). The core circuit area and the estimated operation speed were 1.44 mm^2 and 20 MHz, respectively.

6 Low power design and technology: A power optimized design methodology for low-distortion sigma-delta-pipeline ADCs
Vahid Majidzadeh, Omid Shoaei
April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**
Publisher: ACM Press
Full text available: pdf(2.04 MB) Additional Information: full citation, abstract, references, index terms

A power optimized design methodology for low-distortion sigma-delta-pipeline ADCs is presented. The minimum power consumption of these converters for a given specification has achieved by dynamically exploiting the slewing and partially settling regimes of the integrators, and analytical dynamic expression for maximum possible output swing of the OTAs, which are affected by scaling factors. The proposed, precise, and yet simple

approach gives in rapid and efficient design of ADCs. In order to ve ...

Keywords: power optimization, reduced-sample-rate architectures, sigma-delta-pipeline ADCs

7 Circuits for low power wireless: A novel continuous-time common-mode feedback for low-voltage switched-OPAMP

M. Ali-Bakhshian, K. Sadeghi

August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(572.94 KB) Additional Information: full citation, abstract, references, index terms

A novel rail-to-rail and fast continuous-time common-mode feedback (CMFB) strategy is presented proper for low-voltage Switched-OPAMP (SO) circuits. The threshold voltage change due to bulk signal is used to measure the output voltage. To satisfy speed requirements, averaging common-mode (CM) level and amplifying error signal are realized in a single block. Finally, the measured CM level is controlled by applying an error-voltage dependent current to the output nodes. As a design example, a modi ...

Keywords: CMFB, continuous-time, delta-sigma, low-voltage, switched-OPAMP

8 Simulating sigma-delta modulators in AWEswit

Richard J. Trihy, Ronald A. Rohrer

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(419.72 KB) Additional Information: full citation, references

9 A sigma-delta modulation based BIST scheme for mixed-signal circuits

Jiun-Lang Huang, Kwang-Ting Cheng

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(117.31 KB) Additional Information: full citation, references, citings

10 A BIST scheme for on-chip ADC and DAC testing

Jiun-Lang Huang, Chee-Kian Ong, Kwang-Ting Cheng

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: ACM Press

Full text available: pdf(114.67 KB) Publisher Site Additional Information: full citation, references, citings, index terms

11 A low power high performance switched-current multiplier

D. M. W. Leenaerts, G. H. M. Joordens, J. A. Hegt

August 1996 **Proceedings of the 1996 international symposium on Low power electronics and design**

Publisher: IEEE Press
Full text available: pdf(77.12 KB) Additional Information: full citation, references, index terms

12 Theory of PLL fractional-N frequency synthesizers
A. Marques, M. Steyaert, W. Sansen
January 1998 **Wireless Networks**, Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(482.69 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an overview of the evolution of frequency synthesizers based on phase-locked loops (PLLs). The main limitations of the digital PLLs are described, and the consequent necessity of using fractional-N techniques is justified. The origin of the typical spurious noise lines on the sidelobes of the synthesized frequency is explained. It is shown how to eliminate these spurious noise lines by using digital \Delta\Sigma modulators to control the frequency division value. Finally ...

13 Modeling for analog circuits: Analog circuit behavioral modeling via wavelet collocation method with auto-companding
Jian Wang, Jun Tao, Xuan Zeng, Charles Chiang, Dian Zhou
January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**
Publisher: IEEE Press , IEEE Press
Full text available: pdf(237.36 KB) Publisher Site Additional Information: full citation, abstract, references

In this paper, we propose an auto-companding technique for the analog behavioral modeling via wavelet collocation method. The companding function is automatically constructed according to the singularities of the input-ouput function of the circuit block. Such a general-purpose technique can be applied for the automatic modeling of arbitrary building block of arbitrary input-output function. Moreover, compared with the published modeling approaches, this method works more efficiently in reducing ...

14 Noise considerations for mixed-signal RF IC transceivers
Sayfe Kiaei, David Allstot, Ken Hansen, Nishath K. Verghese
January 1998 **Wireless Networks**, Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(629.05 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses design trade-offs for mixed-signal radio frequency integrated circuit (RF IC) transceivers for wireless applications in terms of noise, signal power, receiver linearity, and gain. During air wave transmission, the signal is corrupted by channel noise, adjacent interfering users, image signals, and multi-path fading. Furthermore, the receiver corrupts the incoming signal due to RF circuit non-linearity (intermodulation), electronic device noise, and digital switching noi ...

15 Wireless telecom silicon integration: analog design for radio, baseband and speech spectrum
J. Sevenhans, D. Haspeslagh, J. Wenin
January 1998 **Wireless Networks**, Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(324.74 KB) Additional Information: full citation, abstract, references, citings, index terms

The application today, pushing analog design for CMOS and RF-bipolar into new frontiers is definitely the mobile radio telephony. New telecom systems like GSM, PCN, DECT, DCS, Wireless in the loop...are all developing very rapidly and will enable us very soon to organise a complete telephone network with full coverage for your car, as well as in your kitchen and on your office desk. In Europe the major telecom companies have worked together to establish one common standard for cellular mobi ...

16 Keynote speech 4: Low power RF IC design for wireless communication

Domine M.W. Leenaerts

August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, index terms

In this paper, the many issues around the system and circuit design of advanced RF front ends for wireless RF applications will be discussed. After a short discussion on technology related issues, design choices linked to the different circuit/system solutions will be discussed.

Keywords: LNA, PLL, RF, VCO, low power, technology, transceivers, wireless communication

17 Mixed analog-digital design: On the dynamic behavior of a novel digital-only sigma--delta A/D converter

Marcel Jacomet, Josef Goette, Venanz Zbinden, Christian Narvaez

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Publisher: ACM Press

Full text available: pdf(293.94 KB) Additional Information: full citation, abstract, references, index terms

Conventional sigma-delta (ΣΔ) analog-to-digital (Ad) converters are based on an analog ΣΔ modulator followed by a digital filter. In this paper we propose a new architecture of a first-order ΣΔ modulator that needs *no active* analog components. We call this ΣΔ modulator "digital-only," and implement with it Ad converters in Fpga's or directly in the software of microprocessors. We here discuss aspects of the dynamic behavio ...

Keywords: ΣΔ modulator, A/D converter, FPGA

18 From System Specification To Layout: Seamless Top-Down Design Methods for Analog and Mixed-Signal Applications

R. Sommer, I. Rugen-Herzig, E. Hennig, U. Gatti, P. Malcovati, F. Maloberti, K. Einwich, C. Clauss, P. Schwarz, G. Noessing

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(462.49 KB) Publisher Site Additional Information: full citation, abstract, citings

Deisgn automation for analog/mixed-signal (A/MS) circuits and systems is still lagging behind compared to what has been reached in the digital area.As System-on-Chip (SoC) designs include analog components in more cases, these analog parts become even more a bottle neck in the overall design process.The paper is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+.Main focus will be the development of seamless top-down design methods for integrated analog and misx-signal syste ...

19 A new quality estimation methodology for mixed-signal and analogue ICs

T. Olbrich, I. A. Grout, Y. E. Aimine, A. M. Richardson, J Contensou

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Publisher: IEEE Computer Society

Full text available: pdf(953.43 KB) Publisher Site Additional Information: full citation, abstract

IC product quality is commonly described as the faulty device level at shipment and is becoming an increasingly important metric in the Microelectronics Industry. This paper presents and demonstrates a quality estimation approach based on Inductive Fault Analysis for mixed-signal and analogue ICs, that quantitatively models the quality related parameters prior to production. It is shown how the approach can be used to optimise the manufacturing test program.

Keywords: IC product quality, analogue ICs, inductive fault analysis, manufacturing test program, mixed-signal ICs, quality control, quality estimation methodology, quality related parameters

20 Interactive presentations: Multi-sensor configurable platform for automotive applications

L. Serafini, F. Carrai, T. Ramacciotti, V. Zolesi

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Designers' forum DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(163.52 KB) Additional Information: full citation, abstract, references

This paper presents a configurable and generic platform architecture suitable to interface several kinds of sensors for automotive applications. A platform-based design approach is pursued to reduce time-to-market. The platform is essentially a library of hardware and software reconfigurable resources. It is based on a microprocessor core plus a set of analog and digital peripherals dedicated to signal acquisition, data processing, storage and transmission. A particular instance of this platform ...

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Terms used **delta sigma falling**

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1 New stability criteria for the design of low-pass sigma-delta modulators
J. A. E. P. van Engelen, R. J. van de Plassche
August 1997 **Proceedings of the 1997 international symposium on Low power electronics a**
Publisher: ACM Press
Full text available: pdf(506.95 KB) Additional Information: full citation, references, citings

2 A Methodology for Designing Continuous-Time Sigma-Delta Modulators
Philippe Benabes, Mansour Keramat, Richard Kielbasa
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Publisher: IEEE Computer Society
Full text available: pdf(534.46 KB) Publisher Site Additional Information: full citation, abstract

A methodology for analysis and synthesis of lowpass sigma-delta (/spl Sigma//spl Delta/) conve permits to synthesize /spl Sigma//spl Delta/ modulators employing continuous-time filters from method is based on the discretization of continuous-time model and using a discrete simulator w simulator. Finally, a realistic design of a second-order /spl Sigma//spl Delta/ modulator wit ...

Keywords: sigma-delta modulation, design methodology, continuous-time sigma-delta modula topology, discrete simulation, low-pass second-order /spl Sigma//spl Delta/ modulator, compen

3 Plagiarism monitoring and detection - towards an open discussion
Edward L. Jones
March 2001 **Journal of Computing Sciences in Colleges**, Volume 16 Issue 3
Publisher: Consortium for Computing Sciences in Colleges , Consortium for Computing Sciences in Colleges
Full text available: pdf(69.40 KB) Additional Information: full citation, abstract, references, cit

Plagiarism in programming courses is a pervasive and frustrating problem that undermines the the gray area separating profitable peer-peer collaboration, excessive dependence on others, ar compelling, pursuing suspected plagiarism is generally not worth the emotional and legal risks t proposes a metrics-based approach to monitoring patterns of similarities among stu ...

4 Metrics based plagarism monitoring
Edward L. Jones
April 2001 **Journal of Computing Sciences in Colleges , Proceedings of the sixth annua journal of computing in small colleges**, Volume 16 Issue 4
Publisher: Consortium for Computing Sciences in Colleges , Consortium for Computing Sciences in Colleges

Full text available: pdf(77.38 KB) Additional Information: full citation, abstract, references, cit

Plagiarism in programming courses is a pervasive and frustrating problem that undermines the (difficult because of the fuzzy boundary between allowable peer-peer collaboration and plagiarisn attendant emotional and legal risks to the student and teacher, with the teacher bearing the bu metrics-based system for monitoring similarities between programs and for gathering the &ld ...

5 Software aids for microprogram development

Christopher Vickery
September 1974 **Conference record of the 7th annual workshop on Microprogramming**
Publisher: ACM Press
Full text available: pdf(296.00 KB) Additional Information: full citation, abstract, references, cit

Debugging of microprograms can be approached in three ways: (1) with the aid of hardware tes debugging programs, and (3) through simulation techniques. This paper discusses these three n debugging program and a simulator developed for debugging microprograms for the Interdata n

6 A behavioral simulation tool for continuous-time ΔΣ modulators

K. Francken, M. Vogels, E. Martens, G. Gielen
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-**
Publisher: ACM Press
Full text available: pdf(219.11 KB) Additional Information: full citation, abstract, references, cit

Circuit--level simulation of ΔΣ modulators is a time--consuming task (taking one or more days f great variety of techniques and tools that speed up the simulations for discrete--time (DT) ΔΣ m implemented in a tool to efficiently simulate and design the continuous--time (CT) counterpart. and/or very high--speed demands for A--to--D converters, desi ...

7 Efficient and accurate testing of analog-to-digital converters using oscillation-test method

K. Arabi, B. Kaminska
March 1997 **Proceedings of the 1997 European conference on Design and Test**
Publisher: IEEE Computer Society
Full text available: pdf(511.01 KB) Publisher Site Additional Information: full citation, abstract, citings

This paper describes a practical test approach for analog-to-digital converters (ADCs) based on test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (Q should be supplied and therefore the need for a costly precision signal generato ...

Keywords: A/D convertor, ADC conversion rate, ADC testing, analog-to-digital converters, anal nonlinearity, digital circuitry, integral nonlinearity, oscillation-test method, quantization band ed

8 Theory of PLL fractional-N frequency synthesizers

A. Marques, M. Steyaert, W. Sansen
January 1998 **Wireless Networks**, Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(482.69 KB) Additional Information: full citation, abstract, references, inc

This paper presents an overview of the evolution of frequency synthesizers based on phase-lock digital PLLs are described, and the consequent necessity of using fractional-N techniques is justi lines on the sidelobes of the synthesized frequency is explained. It is shown how to eliminate th \Delta\Sigma modulators to control the frequency division value. Finally ...

9 New test methods targeting non-classical faults: Embedded software-based self-testing for

A. Krstic, W. C. Lai, K. T. Cheng, L. Chen, S. Dey

June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, inc

At-speed testing of high-speed circuits is becoming increasingly difficult with external testers du tester performance, growing cost of high-performance testers and increasing yield loss caused b empowering the chip to test itself seems like a natural solution. Hardware-based self-testing tec and area overhead and problems caused by the application of non-functional patterns. ...

Keywords: SoC test, VLSI test, functional test, microprocessor test

10 An analysis of selected computer interchange color spaces
James M. Kasson, Wil Plouffe
October 1992 **ACM Transactions on Graphics (TOG)**, Volume 11 Issue 4
Publisher: ACM Press
Full text available: pdf(8.77 MB) Additional Information: full citation, abstract, references, cit

Important standards for device-independent color allow many different color encodings. This fre choose the color space in which to represent their data. A device-independent interchange color colorimetric color representation, ability to encode all visible colors, compact representation for for transforms to and from device-dependent spaces. The performance of CIE 1931 ...

Keywords: CIE 1931 XYZ, CIELAB, CIELUV, SMPTE-C RGB, YCbCr, YES, color, color models, co quantization

11 ACM SIGOIS worldwide membership directory
April 1995 **ACM SIGOIS Bulletin**, Volume 15 Issue SI
Publisher: ACM Press
Full text available: pdf(4.34 MB) Additional Information: full citation, index terms

12 Advanced simulation techniques: Fast and accurate behavioral simulation of fractional-N fr circuits
Michael H. Perrott
June 2002 **Proceedings of the 39th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(2.41 MB) Additional Information: full citation, abstract, references, cit

Techniques for fast and accurate simulation of fractional-N synthesizers at a detailed behavioral uniform time step to be used for the simulator, and can be applied to a variety of phase locked l circuits beyond fractional-N synthesizers, as well as to a variety of simulation frameworks such a a custom C++ simulator are shown to compare well to measured results from a prot ...

Keywords: DLL, PLL, delta, fractional-N, frequency, sigma, synthesizer

13 Experiments with the M & N tree-searching program
James R. Slagle, John K. Dixon
March 1970 **Communications of the ACM**, Volume 13 Issue 3
Publisher: ACM Press
Full text available: pdf(896.52 KB) Additional Information: full citation, abstract, references, cit

The M & N procedure is an improvement to the mini-max backing-up procedure widely used in c

other purposes. It is based on the principle that it is desirable to have many options when maki mini-max procedure assigns to a MAX (MIN) node the value of the highest (lowest) valued succ assigns to a MAX (MIN) node some function of the M (N) highest (lowest) valued succes ...

Keywords: LISP, artificial intelligence, backing-up procedures, decision theory, game playing, h up procedure, tree searching

14 High dynamic range imaging

Paul Debevec, Erik Reinhard, Greg Ward, Sumanta Pattanaik

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**

Publisher: ACM Press

Full text available: pdf(20.22 MB) Additional Information: full citation, abstract

Current display devices can display only a limited range of contrast and colors, which is one of t processing, and display techniques use no more than eight bits per color channel. This course o range imaging, from capture to display, that remove this restriction, thereby enabling images tc range of the original scene rather than the limited subspace imposed by current monitor ...

15 Frontmatter (TOC, Letters, Election results, Software Reliability Resources!, Computing Cu Engineering Volume SE2004, Software Reuse Research, ICSE 2005 Forward)

July 2005 **ACM SIGSOFT Software Engineering Notes**, Volume 30 Issue 4

Publisher: ACM Press

Full text available: pdf(6.19 MB) Additional Information: full citation, index terms

16 Virtual terminal management in a multiple process environment

Keith A. Lantz, Richard F. Rashid

December 1979 **Proceedings of the seventh ACM symposium on Operating systems principl**

Publisher: ACM Press

Full text available: pdf(880.43 KB) Additional Information: full citation, abstract, references, cit

Rochester's Intelligent Gateway provides its users with the facilities for communicating simultan spread out among various computer systems. We have adopted the philosophy that the user sh concurrent tasks or jobs, viewing their output on his display device as he desires. To achieve thi System (VTMS) converts a single physical terminal into multiple virtual terminals

17 Circuit-level optimizations: A probabilistic framework for power-optimal repeater insertion ir variations

Vineet Wason, Kaustav Banerjee

August 2005 **Proceedings of the 2005 international symposium on Low power electronic**

Publisher: ACM Press

Full text available: pdf(395.23 KB) Additional Information: full citation, abstract, references, inc

This paper addresses the problem of power dissipation during the buffer insertion phase of inter nanometer scale designs taking all significant parameter variations into account. The relative eff environmental variations on delay and different components of power has been studied. A probz interconnect designs under variations has been presented and results are compared with those

Keywords: buffer-interconnect system, parameter variations, sensitivity analysis, statistical de

18 A unified approach to test data analysis

Michael A. Gianfagna

June 1978 **Proceedings of the 15th conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(581.18 KB) Additional Information: full citation, abstract, references, cit

To provide cost-effective performance evaluation or engineering feedback from circuit test resul performed on large volumes of non-standard data. Using a large scale data management systen to cope with the above requirements has been developed. TDAS (Test Data Analysis System) ha test data analysis problems which might have been intractable by other means.

19 ANSWERS: A hydrologic / water quality simulator for watershed research

David B. Beasley, Larry F. Huggins

December 1978 **Proceedings of the 10th conference on Winter simulation - Volume 2**

Publisher: IEEE Computer Society Press

Full text available: pdf(810.61 KB) Additional Information: full citation, abstract, references, inc

In recent years, a greatly increased emphasis has been placed on improving and maintaining th Agencies and individuals from both within and without the various levels of government are seel land use, management, and conservation practices or structures might have on the quality and non-agricultural watersheds. ANSWERS (Areal Nonpoint Source Watershed E ...

20 Testing: An efficient linearity test for on-chip high speed ADC and DAC using loop-back

Ji Hwan (Paul) Chun, Hak-soo Yu, Jacob A. Abraham

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Publisher: ACM Press

Full text available: pdf(147.21 KB) Additional Information: full citation, abstract, references, inc

Our method extracts the linearity of on-chip high speed data converters with minimum area ove presence of noise, differential nonlinearities (DNLs) and integral nonlinearities (INLs) of analog-t analog converters (DACs) can be extracted by the proposed method. Our approach exploits the due to noise is distorted by nonlinearities of the ADC, but not by those of the DAC. We fir ...

Keywords: ADC, BIST, DAC, linearity, mixed signal test

Results 1 - 20 of 62 Result page: **1** 2 3 4 next